Intel® Pentium® D Processor 900 Δ Sequence and Intel® Pentium® Processor Extreme Edition 955 Δ

Specification Update

- On 65 nm Process in the 775-land LGA Package and supporting Intel® Extended Memory 64 Technology Φ, and supporting Intel® Virtualization Technology ±

January 2006

Notice: The Intel® Pentium® processor Extreme Edition 955 and Intel® Pentium® D processor 900 sequence may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel® Pentium® Processor Extreme Edition 955 and Intel® Pentium® D Processor 900 Sequence may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

[1]Hyper-Threading Technology requires a computer system with an Intel® processor supporting HT Technology and a Hyper-Threading Technology enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. See <<http://www.intel.com/info/hyperthreading/>> for more information including details on which processors support HT Technology.

Φ Intel® Extended Memory 64 Technology (Intel® EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending on your hardware and software configurations. See www.intel.com/info/em64t for more information including details on which processors support EM64T or consult with your system vendor for more information.

±Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and for some uses, certain platform software enabled for it. Functionality, performance or other benefit will vary depending on hardware and software configurations. Intel Virtualization Technology-enabled BIOS and VMM applications are currently in development.

ΔIntel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. Over time processor numbers will increment based on changes in clock, speed, cache, FSB, or other features, and increments are not intended to represent proportional or quantitative increases in any particular feature. Current roadmap processor number progression is not necessarily representative of future roadmaps. See www.intel.com/products/processor_number for details.

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Enhanced HALT State (C1E) and Enhanced Intel SpeedStep® Technology (EIST) for specified units of this processor available Q2/06. See the Processor Spec Finder at http://processorfinder.intel.com or contact your Intel representative for more information.

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Revision History

Version	Description	Date
-001	• Initial release	December 2005
-002	• Added Intel Pentium D processor 900 sequence specifications	January 2006

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
Intel® Pentium® D Processor 900 Sequence and Intel® Pentium® Processor Extreme Edition 955 Datasheet	310306-002

Related Documents

Document Title	Document Number
IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture, document 253665	http://developer.intel.com/design/pentium4/manuals/index_new.htm
IA-32 Intel® Architecture Software Developer's Manual Volume 2A: Instruction Set Reference Manual A–M, document 253666	http://developer.intel.com/design/pentium4/manuals/index_new.htm
IA-32 Intel® Architecture Software Developer's Manual Volume 2B: Instruction Set Reference Manual, N–Z, document 253667	http://developer.intel.com/design/pentium4/manuals/index_new.htm
IA-32 Intel® Architecture Software Developer's Manual Volume 3: System Programming Guide, document 253668	http://developer.intel.com/design/pentium4/manuals/index_new.htm

Nomenclature

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics (e.g., core speed, L2 cache size, package type, etc.) as described in the processor identification information table. Care should be taken to read all notes associated with each S-Spec number

QDF Number is a several digit code that is used to distinguish between engineering samples. These processors are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. The NDA specification update has a processor identification information table that lists these QDF numbers and the corresponding product sample details.

Errata are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.



Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed component steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This item is either new or modified from the previous version of the document.

Note: Each Specification Update item is prefixed with a capital letter to distinguish the product. The key below details the letters that are used in Intel's microprocessor Specification Updates:

A = Intel® Pentium® II processor
B = Mobile Intel® Pentium® II processor
C = Intel® Celeron® processor
D = Intel® Pentium® II Xeon™ processor
E = Intel® Pentium® III processor
F = Intel® Pentium® processor Extreme Edition and Intel® Pentium® D processor
G = Intel® Pentium® III Xeon™ processor
H = Mobile Intel® Celeron® processor at 466/433/400/366/333/300 and 266 MHz
J = Unannounced 64-bit Intel® Xeon™ processor MP
K = Mobile Intel® Pentium® III processor
L = Intel® Celeron® D processor

M = Mobile Intel® Celeron® processor
N = Intel ® Pentium® 4 processor
O = Intel ® Xeon™ processor MP
P = Intel ® Xeon™ processor
Q = Mobile Intel® Pentium® 4 processor supporting Hyper-Threading Technology on 90 nm process technology
R = Intel® Pentium® 4 processor on 90 nm process
S = 64-bit Intel® Xeon™ processor with 800 MHz system bus (1 MB and 2 MB L2 cache versions)
T = Mobile Intel® Pentium® 4 processor-M
U = Unannounced 64-bit Intel® Xeon™ processor MP
V = Mobile Intel® Celeron® processor on .13 Micron Process in Micro-FCPGA Package
W= Intel® Celeron-M processor
X = Intel® Pentium® M processor on 90nm process with 2-MB L2 Cache
Y = Intel® Pentium® M processor
Z = Mobile Intel® Pentium® 4 processor with 533 MHz system bus
AA= Intel® Pentium® processor Extreme Edition and Intel® Pentium® D processor on 65 nm process
AB= Intel® Pentium® 4 processor on 65 nm process

The Specification Updates for the Pentium® processor, Pentium® Pro processor, and other Intel products do not use this convention.

NO	B1	Plan	ERRATA
AA1	X	No Fix	Locks and SMC Detection May Cause the Processor to Temporarily Hang
AA2	X	No Fix	Memory Aliasing of Pages as Uncacheable Memory Type and Write Back (WB) May Hang the System
AA3	X	No Fix	Data Breakpoints on the High Half of a Floating Point Line Split may not be Captured
AA4	X	No Fix	MOV CR3 Performs Incorrect Reserved Bit Checking When in PAE Paging
AA5	X	No Fix	Incorrect Access Controls to MSR_LASTBRANCH_0_FROM_LIP MSR Registers
AA6	X	No Fix	FXRSTOR May Not Restore Non-canonical Effective Addresses on Processors with Intel® Extended Memory 64 Technology (Intel® EM64T) Enabled
AA7	X	No Fix	A Push of ESP that Faults may Zero the Upper 32 Bits of RSP
AA8	X	No Fix	Checking of Page Table Base Address May Not Match the Address Bit Width Supported by the Platform
AA9	X	No Fix	With TF (Trap Flag) Asserted, FP Instruction That Triggers an Unmasked FP Exception May Take Single Step Trap Before Retirement of Instruction
AA10	X	No Fix	BTS(Branch Trace Store) and PEBS(Precise Event Based Sampling) May Update Memory outside the BTS/PEBS Buffer
AA11	X	No Fix	Control Register 2 (CR2) Can be Updated during a REP MOVS/STOS Instruction with Fast Strings Enabled
AA12	X	No Fix	REP STOS/MOVS Instructions with RCX >=2^32 May Cause a System Hang
AA13	X	No Fix	A 64-Bit Value of Linear Instruction Pointer (LIP) May be Reported Incorrectly in the Branch Trace Store (BTS) Memory Record or in the Precise Event Based Sampling (PEBS) Memory Record



NO	B1	Plan	ERRATA
AA14	X	No Fix	Access to an Unsupported Address Range in Uniprocessor (UP) or Dual-processor (DP) Systems Supporting Intel® Virtualization Technology May Not Trigger Appropriate Actions
AA15	X	PlanFix	VM Exit Due to a MOV from CR8 May Cause an Unexpected Memory Access
AA16	X	PlanFix	The Processor May Incorrectly Respond to Machine Checks during VM Entry/Exit Transitions
AA17	X	PlanFix	Power Down Requests May not be Serviced if a Power Down Transition is Interrupted by an In-Target Probe Event in the Presence of a Specific Type of VM Exit
AA18	X	PlanFix	VM EXIT Due to TPR shadow Below Threshold May Improperly Set and Cause "Blocking by STI" actions
AA19	x	No Fix	Two Correctable L2 Cache Errors in Close Proximity May Cause a System Hang
AA20	x	PlanFix	A VM Exit due to SMI or INIT in Parallel with a Pending FP Exception May Not Correctly Clear the Interruptibility State Bits
AA21	x	No Fix	Processor May Hang with a 25% or Less STPCLK# Duty Cycle
AA22	x	PlanFix	Attempting to Use an LDT Entry when the LDTR Has Been Loaded with an Unusable Segment May Cause Unexpected Memory Accesses
AA23	X	No Fix	Machine Check Exceptions May not Update Last-Exception Record MSRs (LERs)
AA24	X	PlanFix	VM Entry/Exit Writes to LSTAR/SYSCALL_FLAG MSR's May Cause Incorrect Data to be Written to Bits [63:32]
AA25	x	No Fix	Writing the Local Vector Table (LVT) when an Interrupt is Pending May Cause an Unexpected Interrupt
AA26	x	PlanFix	At a Bus Ratio of 13:1, RCNT and Address Parity May be Incorrect
AA27	x	No Fix	The Execution of a VMPTRLD Instruction May Cause an Unexpected Memory Access
AA28	X	No Fix	The Execution of VMPTRLD or VMREAD May Cause an Unexpected Memory Access
AA29	x	PlanFix	On a “Failed VM-entry” VM Exit, the VMCS Pointer May have Incorrect Value
AA30	x	PlanFix	During an Enhanced HALT or Enhanced Intel® Speed Step Technology Ratio Transition the System May Hang

Number	B1	SPECIFICATION CHANGES
		There are no Specification Changes in this Specification Update revision.

Number	B1	SPECIFICATION CLARIFICATIONS
		There are no Specification Clarifications in this Specification Update revision.

Number	B1	DOCUMENTATION CHANGES
		There are no Documentation Changes in this Specification Update revision.



General Information

Figure 1. Intel® Pentium® D Processor 900 Sequence on 65 nm Process (Package Top Markings)

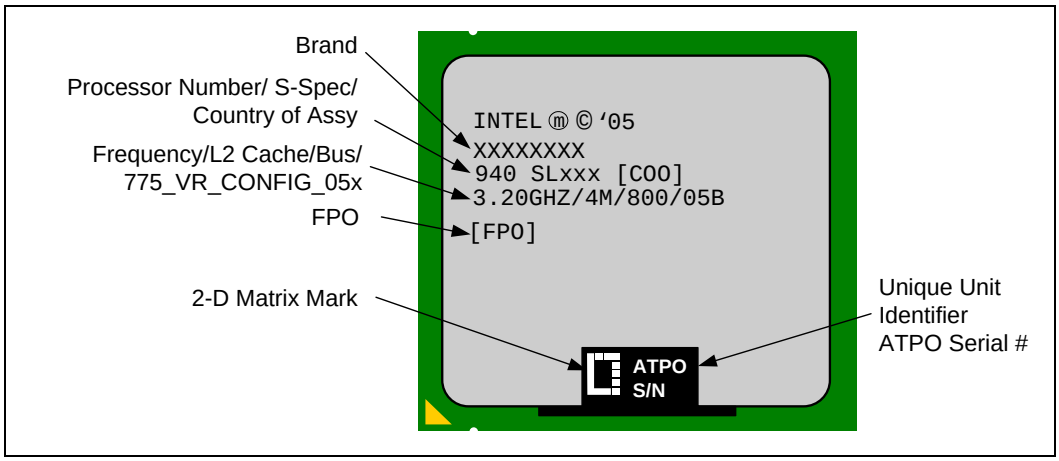
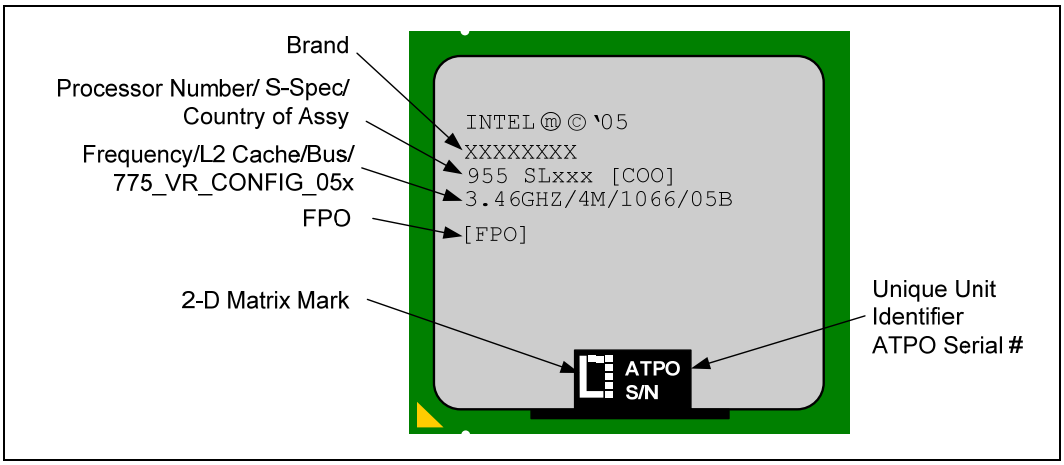


Figure 2. Intel® Pentium® Processor Extreme Edition 955 on 65 nm Process (Package Top Markings)



Identification Information

The Intel® Pentium® processor Extreme Edition 955 and Intel® Pentium® D processor 900 sequence can be identified by the following values:

Family[1]	Model[2]
1111b	1000b

NOTES:
1. The Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
2. The Model corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register. Refer to the *Intel Processor Identification and the CPUID Instruction Application Note* (AP-485).

Table 1. Intel® Pentium® Processor Extreme Edition 955 and Intel® Pentium® D Processor 900 Sequence Identification Information

S-Spec	Core Stepping	L2 Cache Size (bytes)	Processor Signature	Speed Core/Bus	Package and Revision	Notes
QKDH	B1	2M x 2	0F62h	2.80 GHz/800 MHz	775-land FC-LGA46 37.5 x 37.5 mm Rev 01	1, 3
QJZB	B1	2M x 2	0F62h	3 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	1, 3
QJYZ	B1	2M x 2	0F62h	3.2 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 3
QJYX	B1	2M x 2	0F62h	3.4 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 3
QJYW	B1	2M x 2	0F62h	3.46 GHz/1066 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 4
SL8WS	B1	2M x 2	0F62h	2.80 GHz/80 0MHz	775-land FC-LGA46 37.5 x 37.5 mm Rev 01	1, 3
SL8WR	B1	2M x 2	0F62h	3 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	1, 3
SL8WQ	B1	2M x 2	0F62h	3.2 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 3
SL8WP	B1	2M x 2	0F62h	3.4 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 3
SL8WM	B1	2M x 2	0F62h	3.46 GHz/1066 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 4



Table 1. Intel® Pentium® Processor Extreme Edition 955 and Intel® Pentium® D Processor 900 Sequence Identification Information

S-Spec	Core Stepping	L2 Cache Size (bytes)	Processor Signature	Speed Core/Bus	Package and Revision	Notes
SL94S	B1	2M x 2	0F62h	2.80 GHz/80 0MHz	775-land FC-LGA46 37.5 x 37.5 mm Rev 01	1, 5
SL94R	B1	2M x 2	0F62h	3 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	1, 5
SL94Q	B1	2M x 2	0F62h	3.2 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 5
SL94P	B1	2M x 2	0F62h	3.4 GHz/800 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 5
SL94N	B1	2M x 2	0F62h	3.46 GHz/1066 MHz	775-land FC-LGA6 37.5 x 37.5 mm Rev 01	2, 4, 5

NOTES:
1. These processors support the 775_VR_CONFIG_05A (mainstream) specifications.
2. These processors support the 775_VR_CONFIG_05B (performance) specifications.
3. These parts support Enhanced Intel SpeedStep® Technology.
4. These parts support Hyper-Threading Technology.
5. These parts do NOT support Enhanced SpeedStep technology or Enhanced HALT State.

Microcode Updates

Each unique processor stepping/package combination has an associated microcode update that, when applied, constitutes a supported processor (i.e., Specified processor = Processor Stepping + Microcode Update). The proper microcode update must be loaded on each processor in a system. The proper microcode update is defined as the latest production microcode update available from Intel for a given family, model and stepping of the processor. Any processor that does not have the correct microcode update loaded is considered to be operating out of specification. Contact your Intel Field Representative to receive the latest production microcode updates.

Table 2. Intel® Pentium® Processor Extreme Edition 955 and Intel® Pentium® D Processor 900 Sequence Microcode Update Guide

Microcode Update	Customer Release Date	Intended Stepping	Revision ID	Workaround for Errata
M04F620D	11/2005	B-1	0D	AA15, AA18, AA20, AA22, AA24, AA28, AA29. AA30

Table 3. Intel® Pentium® Processor Extreme Edition 955 and Intel® Pentium® D Processor 900 Sequence .PDB File Guide

File Name	Customer Release Date	Supported Steppings	Microcode Updates Included
PER_B_39.EXE	11/2005	B1	M04F620D

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Errata

AA1. Bus Locks and SMC Detection May Cause the Processor to Hang Temporarily

Problem: The processor may temporarily hang in an HT Technology enabled system if one logical processor executes a synchronization loop that includes one or more locks and is waiting for release by the other logical processor. If the releasing logical processor is executing instructions that are within the detection range of the self -modifying code (SMC) logic, then the processor may be locked in the synchronization loop until the arrival of an interrupt or other event.

Implication: If this erratum occurs in an HT Technology enabled system, the application may temporarily stop making forward progress. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA2. Memory Aliasing of Pages As Uncacheable Memory Type and Write Back (WB) May Hang the System

Problem: When a page is being accessed as either Uncacheable (UC) or Write Combining (WC) and WB, under certain bus and memory timing conditions, the system may loop in a continual sequence of UC fetch, implicit writeback, and Request For Ownership (RFO) retries.

Implication: This erratum has not been observed in any commercially available operating system or application. The aliasing of memory regions, a condition necessary for this erratum to occur, is documented as being unsupported in the *IA-32 Intel® Architecture Software Developer's Manual*, Volume 3, section 10.12.4, Programming the PAT. However, if this erratum occurs the system may hang.

Workaround: The pages should not be mapped as either UC or WC and WB at the same time.

Status: For the stepping affected, see the *Summary Tables of Changes.*

AA3. Data Breakpoints on the High Half of a Floating Point Line Split May Not Be Captured

Problem: When a floating point load which splits a 64-byte cache line gets a floating point stack fault, and a data breakpoint register maps to the high line of the floating point load, internal boundary conditions exist that may prevent the data breakpoint from being captured.

Implication: When this erratum occurs, a data breakpoint will not be captured.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA4. MOV CR3 Performs Incorrect Reserved Bit Checking When in PAE Paging

Problem: The MOV CR3 instruction should perform reserved bit checking on the upper unimplemented address bits. This checking range should match the address width reported by CPUID instruction 0x8000008. This erratum applies whenever PAE is enabled.

Implication: Software that sets the upper address bits on a MOV CR3 instruction and expects a fault may fail. This erratum has not been observed with commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA5. Incorrect Access Controls to MSR_LASTBRANCH_0_FROM_LIP MSR Registers

Problem: When an access is made to the MSR_LASTBRANCH_0_FROM_LIP MSR register, an expected #GP fault may not happen.

Implication: A read of the MSR_LASTBRANCH_0_FROM_LIP MSR register may not cause a #GP fault.

Workaround: None Identified

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA6. FXRSTOR May Not Restore Non-canonical Effective Addresses on Processors with Intel® Extended Memory 64 Technology (Intel® EM64T) Enabled

Problem: If an x87 data instruction has been executed with a non-canonical effective address, FXSAVE may store that non-canonical FP Data Pointer (FDP) value into the save image. An FXRSTOR instruction executed with 64-bit operand size may signal a General Protection Fault (#GP) if the FDP or FP Instruction Pointer (FIP) is in non-canonical form.

Implication: When this erratum occurs, Intel EM64T enabled systems may encounter an unintended #GP fault.

Workaround: Software should avoid using non-canonical effective addressing in EM64T enabled processors. BIOS can contain a workaround for this erratum removing the unintended #GP fault on FXRSTOR.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA7. A Push of ESP That Faults May Zero the Upper 32 Bits of RSP

Problem: In the event that a push ESP instruction, that faults, is executed in compatibility mode, the processor will incorrectly zero upper 32-bits of RSP.

Implication: A Push of ESP in compatibility mode will zero the upper 32-bits of RSP. Due to this erratum, this instruction fault may change the contents of RSP. This erratum has not been observed in commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA8. Checking of Page Table Base Address May Not Match the Address Bit Width Supported by the Platform

Problem: If the page table base address, included in the page map level-4 table, page-directory pointer table, page-directory table or page table, exceeds the physical address range supported by the platform (e.g. 36-bit) and it is less than the implemented address range (e.g. 40-bit), the processor does not check if the address is invalid.

Implication: If software sets such invalid physical address in those tables, the processor does not generate a page fault (#PF) upon access to that virtual address, and the access results in an incorrect read or write. If BIOS provides only valid physical address ranges to the operating system, this erratum will not occur.

Workaround: BIOS must provide valid physical address ranges to the operating system.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA9. With TF (Trap Flag) Asserted, FP Instruction That Triggers an Unmasked FP Exception May Take Single Step Trap before Retirement of Instruction

Problem: If an FP instruction generates an unmasked exception with the EFLAGS.TF=1, it is possible for external events to occur, including a transition to a lower power state. When resuming from the lower power state, it may be possible to take the single step trap before the execution of the original FP instruction completes.

Implication: A Single Step trap will be taken when not expected.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.



AA10. BTS(Branch Trace Store) and PEBS(Precise Event Based Sampling) May Update Memory outside the BTS/PEBS Buffer

Problem: If the BTS/PEBS buffer is defined such that:

- The difference between BTS/PEBS buffer base and BTS/PEBS absolute maximum is not an integer multiple of the corresponding record sizes
- BTS/PEBS absolute maximum is less than a record size from the end of the virtual address space
- The record that would cross BTS/PEBS absolute maximum will also continue past the end of the virtual address space

A BTS/PEBS record can be written that will wrap at the 4G boundary (IA32) or 2^64 boundary (EM64T mode), and write memory outside of the BTS/PEBS buffer.

Implication: Software that uses BTS/PEBS near the 4G boundary (IA32) or 2^64 boundary (EM64T mode), and defines the buffer such that it does not hold an integer multiple of records can update memory outside the BTS/PEBS buffer.

Workaround: Define BTS/PEBS buffer such that BTS/PEBS absolute maximum minus BTS/PEBS buffer base is integer multiple of the corresponding record sizes as recommended in the IA-32 Intel® Architecture Software Developer's Manual, Volume 3.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA11. Control Register 2 (CR2) Can be Updated during a REP MOVS/STOS Instruction with Fast Strings Enabled

Problem: Under limited circumstances while executing a REP MOVS/STOS string instruction, with fast strings enabled, it is possible for the value in CR2 to be changed as a result of an interim paging event, normally invisible to the user. Any higher priority architectural event that arrives and is handled while the interim paging event is occurring may see the modified value of CR2.

Implication: The value in CR2 is correct at the time that an architectural page fault is signaled. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA12. REP STOS/MOVS Instructions with RCX >=2^32 May Cause a System Hang

Problem: In IA-32e mode using Intel EM64T-enabled processors, executing a repeating string instruction with the iteration count greater than or equal to 2^32 and a pending event may cause the REP STOS/MOVS instruction to live lock and hang.

Implication: When this erratum occurs, the processor may live lock and result in a system hang. Intel has not observed this erratum with any commercially available software.

Workaround: Do not use strings larger than 4 GB.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA13. A 64-Bit Value of Linear Instruction Pointer (LIP) May be Reported Incorrectly in the Branch Trace Store (BTS) Memory Record or in the Precise Event Based Sampling (PEBS) Memory Record

Problem: On a processor supporting Intel® EM64T,

- If an instruction fetch wraps around the 4G boundary in Compatibility Mode, the 64-bit value of LIP in the BTS memory record will be incorrect (upper 32 bits will be set to FFFFFFFFh when they should be 0).
- If a PEBS event occurs on an instruction whose last byte is at memory location FFFFFFFFh, the 64-bit value of LIP in the PEBS record will be incorrect (upper 32 bits will be set to FFFFFFFFh when they should be 0).

Implication: Intel has not observed this erratum on any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes*.

AA14. Access to an Unsupported Address Range in Uniprocessor (UP) or Dual-processor (DP) Systems Supporting Intel® Virtualization Technology May Not Trigger Appropriate Actions

Problem: When using processors supporting Intel® Virtualization Technology and configured as dual- or single-processor-capable (i.e. not multiprocessor-capable), the processor should perform address checks using a maximum physical address width of 36. Instead, these processors will perform address checks using a maximum physical address width of 40.

Implication: Due to this erratum, actions which are normally taken upon detection of an unsupported address may not occur. Software which does not attempt to access unsupported addresses will not experience this erratum.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes.*



AA15. VM Exit Due to a MOV from CR8 May Cause an Unexpected Memory Access

Problem: In a system supporting Intel® Virtualization Technology and Intel® Extended Memory 64 Technology, if the "CR8-store exiting" bit in the processor-based VM-execution control field is set and the "use TPR shadow" bit is not set, a MOV from CR8 instruction executed by a Virtual Machine Extensions (VMX) guest that causes a VM exit may generate an unexpected memory access.

Implication: When this erratum occurs, a read access to unexpected address may be issued to the chipset. Subsequent side effects are dependent on chipset operation and may include system hang.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA16. The Processor May Incorrectly Respond to Machine Checks during VM Entry/Exit Transitions

Problem: In systems supporting Intel® Virtualization Technology, when machine checks are encountered during VM entry/exit transitions, the processor is expected to respond with a VM exit (if a machine check occurs during VM entry) or abort (if a machine check occurs during VM exit). As a result of this erratum when machine checks occur during VM entry/exit transitions the processor will attempt to service the machine check which may lead to IERR-shutdown or execution of the Machine Check handler, dependent on the CR4.MCE setting.

Implication: The system may end up in the shutdown state if CR4.MCE is not set.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA17. Power Down Requests May not be Serviced if a Power Down Transition is Interrupted by an In-Target Probe Event in the Presence of a Specific Type of VM Exit

Problem: In a system supporting Intel® Virtualization Technology, the processor may service a pended VM exit prior to completely exiting out of a low power state when the following sequences of events occur:

- Chip-wide power down transition occurs and
- VM exit due to a VMLaunch, VMResume, STI, POPF, POPFD, or IRET instruction is pended and
- Chip-wide power down transition is interrupted by an In-Target Probe event.

Implication: Due to this erratum the processor may not recognize further STPCLK# assertions, TM1, TM2, or Enhanced Intel SpeedStep® technology. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA18. VM EXIT Due to TPR shadow Below Threshold May Improperly Set and Cause "Blocking by STI" actions

Problem: In a system supporting Intel® Virtualization Technology and Intel® EM64T, the “blocking by STI” bit of the interruptibility-state field may be saved as 1 rather than 0. This erratum may occur when a STI instruction is executed directly prior to a MOV to CR8 which results in a VM exit due to a reduction of the TPR shadow value below the TPR threshold.

Implication: When this erratum occurs, delivery of an interrupt may be delayed by one instruction.

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA19. Two Correctable L2 Cache Errors in Close Proximity May Cause a System Hang

Problem: If two correctable L2 cache errors are detected in close proximity to each other, a livelock may occur as a result of the processor being unable to resolve this condition.

Implication: When this erratum occurs, the processor may livelock and result in a system hang. Intel has only observed this erratum while injecting cache errors in simulation..

Workaround: None identified.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA20. A VM Exit due to SMI or INIT in Parallel with a Pending FP Exception May Not Correctly Clear the Interruptibility State Bits



Problem: When a pending FP exception is ready to be taken, a VM exit due to SMI or INIT may not clear Blocking by STI and/or Blocking by MOV SS bits correctly in Virtual-Machine Control Structure (VMCS) as expected..

Implication: A VM exit due to SMI or INIT may show incorrect STI and/or MOV SS blocking state in VM-exit Interruptibility field..

Workaround: It is possible for the BIOS to contain a workaround for this erratum. .

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA21. Processor May Hang with a 25% or Less STPCLK# Duty Cycle

Problem: If a system de-asserts STPCLK# at a 25% or less duty cycle and the processor thermal control circuit (TCC) on-demand clock modulation is active, the processor may hang. This erratum does not occur under the automatic mode of the TCC.

Implication: When this erratum occurs, the processor may hang.

Workaround: If use of the on-demand mode of the processor's TCC is desired in conjunction with STPCLK# modulation, then assure that STPCLK# is not asserted at a 25% duty cycle.

Status: For the steppings affected, see the Summary Tables of Changes.

AA22. Attempting to Use an LDT Entry when the LDTR Has Been Loaded with an Unusable Segment May Cause Unexpected Memory Accesses

Problem: In a system supporting Intel® Virtualization Technology, the processor may incorrectly VM exit under the following conditions:

1. Interrupt-Window-Exiting VM-execution control is set
2. RFLAGS[IF]=1
3. Chipwide Powerdown transition requests occur when the processor is in Wait-For-SIPI or Shutdown states

Implication: Due to this erratum, Interrupt-Window-Exiting VM exits may take the logical processor out of Wait-For-SIPI and Shutdown states. Intel has not observed this erratum with any commercially available software.

Workaround: It is possible for the BIOS to contain a workaround for this erratum

Status: For the steppings affected, see the Summary Tables of Changes.

AA23. Machine Check Exceptions May not Update Last-Exception Record MSRs (LERs)

Problem: The Last-Exception Record MSRs (LERs) may not get updated when Machine Check Exceptions occur

Implication: When this erratum occurs, the LER may not contain information relating to the machine check exception. They will contain information relating to the exception prior to the machine check exception.

Workaround: None identified

Status: For the steppings affected, see the Summary Tables of Changes.

AA24. VM Entry/Exit Writes to LSTAR/SYSCALL_FLAG MSR's May Cause Incorrect Data to be Written to Bits [63:32]

Problem: Incorrect MSR data in bits [63:32] may be observed in the following two cases:

1. When ECX contains 0xC0000084 and a VM entry/exit writes the IA32_CR_LSTAR MSR (MSR Address 0xC0000082) bits [63:32] of the data may be zeroed
2. When ECX does not contain 0xC0000084 and a VM entry/exit writes the IA32_CR_SYSCALL_FLAG_MASK MSR (MSR Address 0xC0000084) bits [63:32] of the data may not be zeroed

Implication: Bits [63:32] of the affected MSRs may contain the wrong data after a VM exit/entry which loads the affected MSR.

Workaround: It is possible for the BIOS to contain a workaround for this erratum

Status: For the steppings affected, see the Summary Tables of Changes.

AA25. Writing the Local Vector Table (LVT) when an Interrupt is Pending May Cause an Unexpected Interrupt

Problem: If a local interrupt is pending when the LVT entry is written, an interrupt may be taken on the new interrupt vector even if the mask bit is set.

Implication: An interrupt may immediately be generated with the new vector when a LVT entry is written, even if the new LVT entry has the mask bit set. If there is no Interrupt Service Routine (ISR) set up for that vector the system will GP fault. If the ISR does not do an End of Interrupt (EOI) the bit for the vector will be left set in the in-service register and mask all interrupts at the same or lower priority.

Workaround: Any vector programmed into an LVT entry must have an ISR associated with it, even if that vector was programmed as masked. This ISR routine must do an EOI to clear any unexpected interrupts that may occur. The ISR associated with the spurious vector does not generate an EOI, therefore the spurious vector should not be used when writing the LVT.

Status: For the steppings affected, see the *Summary Tables of Changes.*



AA26. At a Bus Ratio of 13:1, RCNT and Address Parity May be Incorrect

Problem: In a system running at the 13:1 bus ratio, RCNT[0] (ADDR# [28], phase b) may report incorrect information.

Implication: RCNT[0] may contain incorrect information and cause address parity machine check errors.

Workaround: Address parity should be disabled and RCNT information should be ignored at the bus ratio of 13:1.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA27. The Execution of a VMPTRLD Instruction May Cause an Unexpected Memory Access

Problem: In a system supporting Intel® Virtualization Technology, executing VMPTRLD may cause a memory access to an address not referenced by the memory operand.

Implication: This erratum may cause unpredictable system behavior including system hang.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA28. The Execution of VMPTRLD or VMREAD May Cause an Unexpected Memory Access

Problem: On processors supporting Intel® Virtualization Technology, executing a VMPTRLD or a VMREAD instruction outside of VMX mode may result in a load to an unexpected address.

Implication: This erratum may cause a load to an unexpected memory address.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA29. On a “Failed VM-entry” VM Exit, the VMCS Pointer May have Incorrect Value

Problem: On a “failed VM-entry” VM exit, the VMCS pointer may have incorrect value.

Implication: The value of the VMCS pointer may be incorrect and may result in unpredictable behavior after the "failed VM-entry”.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the *Summary Tables of Changes.*

AA30. During an Enhanced HALT or Enhanced Intel® Speed Step Technology Ratio Transition the System May Hang

Problem: The BNR signal may not function properly during an Enhanced HALT or Enhanced Intel® Speed Step Technology ratio transition.

Implication: The system may hang due to incorrect BNR signaling.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the *Summary Tables of Changes.*

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Specification Changes

The Specification Changes listed in this section apply to the following documents:

- *Intel® Pentium® D Processor 900 Sequence and Intel® Pentium® Processor Extreme Edition 955 Datasheet*

All Specification Changes will be incorporated into a future version of the appropriate Pentium D processor 900 sequence and Pentium processor Extreme Edition 955 documentation.

◭ Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. Over time processor numbers will increment based on changes in clock, speed, cache, FSB, or other features, and increments are not intended to represent proportional or quantitative increases in any particular feature. Current roadmap processor number progression is not necessarily representative of future roadmaps. See www.intel.com/products/processor_number for details.

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Specification Clarifications

The Specification Clarifications listed in this section apply to the following documents:

- *Intel® Pentium® D Processor 900 Sequence and Intel® Pentium® Processor Extreme Edition 955 Datasheet*

All Specification Clarifications will be incorporated into a future version of the appropriate Pentium D processor 900 sequence and Pentium processor Extreme Edition 955 documentation.

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Documentation Changes

The Documentation Changes listed in this section apply to the following documents:

- *Intel® Pentium® D Processor 900 Sequence and Intel® Pentium® Processor Extreme Edition 955 Datasheet*

All Documentation Changes will be incorporated into a future version of the appropriate Pentium D processor 900 sequence and Pentium processor Extreme Edition 955 documentation.

Note: Documentation changes for IA-32 Intel® Architecture Software Developer's Manual volumes 1, 2A, 2B, 3 will be posted in a separate document *IA-32 Intel® Architecture Software Developer's Manual Documentation Changes*. Follow the link below to become familiar with this file.

http://developer.intel.com/design/pentium4/specupdt/252046.htm

There are no documentation changes in this Specification Update revision.

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